REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-69 are pending. Claims 1-69 have been rejected. Claims 1, 8, 9, 11, 13, 15, 19, 34, 41, 42, 44, and 46, 48, 52 and 69 have been objected to.

Claims 1, 8, 9, 11, 13, 15, 19, 34, 41, 42, 44, 46, 48, 52, 68, and 69 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Applicants reserve all rights with respect to the applicability of the Doctrine of Equivalents.

Objections to the Claims

Examiner objected to claims 1, 8, 9, 11, 13, 15, 19, 34, 41, 42, 44, 46, 48, 52, 68, and 69 because of informalities.

Applicants have amended claims 1, 8, 9, 11, 13, 15, 19, 34, 41, 42, 44, 46, 48, 52, 68, and 69.

Therefore, applicants submit that the Examiner's objections with respect to claims 1, 8, 9, 11, 13, 15, 19, 34, 41, 42, 44, 46, 48, 52, 68, and 69 have been overcome.

Claim 68 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicants have amended claim 68.

Therefore, applicants respectfully submit that claim 68 is now allowable under 35 U.S.C. § 112, second paragraph.

Claims 1-2, 5-7, 11-14, 17-20, 23-30, 32-35, 38-40, 44-47, 50-53, 56-63, 65-66, and 68 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,446,198 to Sazegari (hereinafter "Sazegari").

Amended claim 1 reads as follows:

> A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:
> receiving a string of bits;
> selecting a plurality of segments of bits from the string of bits;
> generating a plurality of indices using the plurality of segments of bits from the string of bits;
> receiving a configuration indicator, wherein the configuration indicator indicates how to configure a plurality of look-up units into one or more look-up tables for execution of the single instruction;
> configuring the plurality of look-up units into one or more look up tables according to the configuration indicator;
> looking up simultaneously a plurality of entries from the one or more look-up tables using the plurality of indices, the one or more look-up tables is configured from the plurality of look-up units, wherein each of said plurality of look-up units is a memory unit that is separate and distinct from others of said plurality of look-up units and is individually accessible independent of operations of the other look-up units; and
> combining the plurality of entries into a first result;
> wherein the above operations are performed in response to the microprocessor receiving the single instruction.

(Amended claim 1)(emphasis added)

The Examiner states that "each unit [data 1, data 2) [of Sazegari] is individually accessible independent of operations to other tables."(Office Action, p. 4, 10/19/08). Applicants respectfully disagree.

Sazegari discloses a vectorized table lookup. More specifically, Sazegari discloses:

> In accordance with the invention, this objective is achieved by logically dividing a large table into a number of smaller tables that can be uniquely indexed with a permute instruction. For instance, a 256-byte table can be logically divided into eight 32-byte tables. Each smaller table consists of two data vectors, which constitute the operands for the permute instruction….

(Sazegari, col. 2, lines 17-24)(emphasis added)

In particular, Sazegari discloses the following:

> For table lookup operations, the permute instruction can be used to perform 16 simultaneous lookup operations on a 32-byte entry table. FIG. 4 illustrates such a table 34, which consists of two 16-byte vectors, data1 and data2. Each vector can be stored in one register of the CPU. The permute instruction can be used to simultaneously read 16 values from these two vectors, in accordance with index values in a register 36, and store the 16 output results in sequential order in another register 38.

(Sazegari, col. 2, lines 17-35)(emphasis added)

Thus, Sazegari merely discloses the tables (data 1) and (data 2) (Figures 3-4) that are accessible by the same [permute] operation, in contrast to each of the plurality of look-up units that is a memory unit that is separate and distinct from others of said plurality of look-up units and is individually accessible independent of operations of the other look-up units, as recited in amended claim1.

Further, Sazegari merely discloses logically dividing a large table into a number of smaller tables (Figure 4). In contrast, amended claim 1 refers to receiving a configuration indicator, wherein the configuration indicator indicates how to configure a plurality of look-up units that are into one or more look-up tables for execution of the single instruction, wherein each of the plurality of look-up units is a memory unit that is separate and distinct from others of the plurality of look-up units and is individually accessible independent of operations of the other look-up units; and configuring the plurality of look-up units into one or more look up tables according to the configuration indicator.

Because Sazegari fails to disclose all limitations of amended claim1, applicants respectfully submit that amended claim 1 is not anticipated by Sazegari under 35 U.S.C. § 102(e).

Given that claims 2, 5-7, 11-14, 17-20, 23-30, 32-35, 38-40, 44-47, 50-53, 56-63, 65-66, and 68 contain limitations that are similar to those discussed with respect to amended claim 1, applicants respectfully submit that claims 2, 5-7, 11-14, 17-20, 23-30, 32-35, 38-40, 44-47, 50-53, 56-63, 65-66, and 68 are not anticipated by Sazegari under 35 U.S.C. § 102(e).

Claims 3-4, 8-10, 15-16, 21-22, 31, 36-37, 41-43, 48-49, 54-55, 64, and 69 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sazegari.

As set forth above, Sazegari merely discloses the tables (data 1) and (data 2) (Figures 3-4) that are accessible by the same [permute] operation, in contrast to each of the plurality of look-up units that is a memory unit that is separate and distinct from others of said plurality of look-up units and is individually accessible independent of operations of the other look-up units, as recited in amended claim1.

Additionally, Sazegari merely discloses logically dividing a large table into a number of smaller tables (Figure 4). In contrast, amended claim 1 refers to receiving a configuration indicator, wherein the configuration indicator indicates how to configure a plurality of look-up units that are into one or more look-up tables for execution of the single instruction, wherein each of the plurality of look-up units is a memory unit that is separate and distinct from others of the plurality of look-up units and is individually accessible independent of operations of the other look-up units; and configuring the plurality of look-up units into one or more look up tables according to the configuration indicator.

Given that claims 3-4, 8-10, 15-16, 21-22, 31, 36-37, 41-43, 48-49, 54-55, 64, and 69 contain limitations that are similar to those discussed with respect to amended claim 1,

applicants respectfully submit that claims 3-4, 8-10, 15-16, 21-22, 31, 36-37, 41-43, 48-49, 54-55, 64, and 69 are not obvious under 35 U.S.C. § 103(a) over Sazegari.

Claim 67 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Sazegari in view of U.S. Patent No. 5,526,501 to Shams ("Shams").

It is respectfully submitted that Sazegari does not teach or suggest a combination with Shams, and Shams does not teach or suggest a combination with Sazegari. It would be impermissible hindsight, based on applicants' own disclosure, to combine Sazegari and Shams.

Sazegari teaches a vectorized table lookup (Abstract).

Shams, in contrast, teaches variable accuracy indirect addressing scheme (Abstract).

Furthermore, even if the table lookup of Sazegari were combined with the addressing scheme of Shams, such a combination would still lack receiving a configuration indicator, wherein the configuration indicator indicates how to configure a plurality of look-up units that are into one or more look-up tables for execution of the single instruction, wherein each of the plurality of look-up units is a memory unit that is separate and distinct from others of the plurality of look-up units and is individually accessible independent of operations of the other look-up units; and configuring the plurality of look-up units into one or more look up tables according to the configuration indicator, as recited in amended claim 1.

Given that claim 67 contains limitations that are similar to those discussed with respect to amended claim 1, applicants respectfully submit that claim 67 is not obvious under 35 U.S.C. § 103(a) over Sazegari in view of Shams.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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